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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/032,894
Filing Date: October 26, 2001
Appellant(s): LINDHOLM ET AL.

Sean R. O'Dowd
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/1/2006 appealing from the Office action mailed 3/3/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,184,902	Krech	02-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following ground(s) of rejection are applicable to the appealed claims:

Claims 24-25, 27-29 and 30-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Krech, Jr US patent no. 6,184,902.

Re claim 24, Krech discloses a lighting system for graphics processing (col. 1, lines 48-67), comprising at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom (fig. 5), a multiplication logic unit coupled to the at least one input buffer (fin. 3-element 55), an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit (col. 3. lines 22-34), a register unit coupled to the arithmetic logic unit (col. 14, lines 28-55), and a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit (col. 3. lines 22-34: fins. 3-5);

Wherein lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data (fig. 5; Krech discloses multiplication logic unit with a feedback loop coupled to an input thereof; see col. 11, line 45 to col. 13, line 15, fig. 7 wherein Krech teaches a vertex looping routine is commenced, which processes data associated with a vertex of the primitive during each loop operation. The appropriate control unit logic element determines via the last vertex bit whether the vertex that was recently operated on in the past by the stack is the last vertex of the primitive that is currently at issue). In other words, Krech teaches architecturally, the geometry accelerator includes a plurality of processing elements (e.g., an arithmetic logic unit, a multiplier, a divider, a compare mechanism, a clamp mechanism, etc.) and a plurality of control units (e.g., a transform mechanism, a decomposition mechanism, a clip mechanism, a bow-tie mechanism, a light mechanism, a classify mechanism, a plane equation mechanism, a fog mechanism, etc.) that

utilize the processing elements for performing data manipulations upon image data. In that each of the individual control unit logic elements situated within the control unit logic assists a corresponding control unit in accomplishing branching and indirect addressing. Each of the individual control unit logic elements is configured to make logical decisions for its respective control unit based upon and as a function of state data, including in the preferred embodiment, two least significant bits (LSBs) of the next address from the current instruction of the ROM, the branch field from the current instruction of the ROM, a condition code from the current instruction of the ROM, last vertex and light signals from a vertex/light counter indicative of whether or not the current instruction involves the last vertex and last light to be processed in a grouping of vertices/lights associated with a code subroutine, and the flags from the stack.

Re claim 25, Krech discloses multiplication logic unit has a feedback loop coupled to an input thereof (col. 11, line 45 to col. 13, line 15: fin. 7). In other words, Krech teaches a vertex looping routine is commenced, which processes data associated with a vertex of the primitive during each loop operation. The appropriate control unit logic element determines via the last vertex bit whether the vertex that was recently operated on in the past by the stack is the last vertex of the primitive that is currently at issue.

Re claim 27, Krech discloses arithmetic logic unit and the multiplication logic unit include multiplexers (col. 3. line 15 to col. 4, line 41). Krech teaches in architecture, the geometry accelerator includes a plurality of processing elements (e.g., an arithmetic logic unit, a multiplier, a divider, a compare mechanism, a clamp mechanism, etc.) and a plurality of control units (e.g., a transform mechanism, a decomposition mechanism, a clip mechanism, a bow-tie mechanism, a light mechanism, a classify mechanism, a plane equation mechanism, a fog

mechanism, etc.) that utilize the processing elements for performing data manipulations upon image data. In accordance with the invention, the control units are implemented in a read-only memory (ROM) via micro-code instructions.

Re claims 28-29, Krech discloses multiplication logic unit includes three multipliers coupled in parallel and arithmetic logic includes three adders coupled in series and parallel (col. 5, lines 14-45.. col. 14, lines 13-48: figs. 4-5). In figure 4, Krech discloses the implementation enables multiway logic branching, which further enhances performance. In other words, multiple decisions can be made at the same time and in parallel. Moreover, the data path control field, which is passed to the stack from the ROM on connection, causes the ALU 54 (figure 5) to execute by adding operands A and B. Operands A and B are retrieved from the registers and/or RAM, the location of which is defined in the data path control of the instruction.

Re claims 30 and 34, the limitations of claims 30 and 34 are identical to claim 24 above except for a memory. Therefore, claims 30 and 34 are treated the same as discussed with respect to claim 24 above.

Krech's teaching is a computer graphics systems implemented in a read only memory. It is apparent that a read-only memory is a memory.

Re claim 31, Krech discloses memory includes a plurality of constants for processing the vertex data (col. 14, line 39 to col. 15, line 4).

Re claims 32-33, Krech discloses memory has a read terminal coupled to the multiplication logic unit (fig. 4). Krech teaches Read-only memory. In that he discloses Figure 4 is an electronic block diagram showing a geometry accelerator of the invention having control

units implemented in a read-only memory (ROM) and branch logic configured to assist instruction branching within the ROM.

(10) Response to Argument

On Page 5 in the remarks, the Appellant argued with respect to the claim 24 in substance:

(A) "Krech does not disclose coupling a lighting logic unit and a multiplication logic unit through such a conversion module. In fact, Krech does not even disclose Applicants' claimed conversion module. For example, a simple word search on the Krech patent reveals that it does not once mention any module for converting between scalar vertex data and vector vertex data. Similarly, Krech's figures do not illustrate a conversion module as claimed-much less a lighting logic unit and a multiplication logic unit coupled via a conversion module. Accordingly, Krech cannot be the basis for a proper 35 U.S.C. 102 rejection of claim 24 or the corresponding dependent claims."

In response to the arguments in (A), Krech further teaches in Fig. 5, col. 11, line 45 to col. 13, line 15, Fig. 7, a multiplication logic unit, i.e., MULTIPLIER 55 (See also column 2, lines 35-64 for the background information) within the stack 51 of the operating processing element 52 as shown in Fig. 5. Krech teaches in Fig. 5, col. 11, line 45 to col. 13, line 15, Fig. 7 a control unit logic element 115 (which corresponds to the claim limitation of "a lighting logic unit") coupled to the multiplication logic unit via a conversion module (i.e., the control unit 17 of Fig. 5) which operates the vertex data using the control signals or microcode instruction from the logic unit 115. The control unit includes among other things, the transform mechanism and light

mechanism. In Fig. 5, the TRANSFORM, DECOMP, CLIP, BOW-TIE, LIGHT, FOG mechanisms are clearly shown as being the elements of the conversion module. The conversion module 17 comprises a transform mechanism (TRANS) 24 for performing transformations on the vertex data such as scaling or moving a vertex in space, a decomposition mechanism (DECOMP) for decomposing primitives such as converting a quadrilateral into a triangle and a plane equation mechanism 32 operating on the vertex data via the mathematical operations on the plane equation vector.

Moreover, the appellant relies on the "word search" on the Krech patent for the conversion module. However, Krech discloses in Fig. 5, col. 11, line 45 to col. 13, line 15, Fig. 7 a control unit 17 which operates the vertex data using the control signals or microcode instruction from the logic unit 115 wherein the control unit 17 includes, *inter alia*, a **transform mechanism**, a clipping mechanism, a light mechanism, a decomposition mechanism, and a plane equation mechanism for performing transformations on the vertex data such as **scaling or moving a vertex in space** and for decomposing primitives such as converting a quadrilateral into a triangle and operating on the vertex data via the mathematical operations on the plane equation vector. It is clear that the control unit 17 performs such functionality as **coverting/transforming the vertex data, and scaling the vertex data that converts the vertex data to the vector vertex data**.

The claim 24 also set forth the claim limitation of "a conversion module adapted for converting scalar vertex data to vector vertex data." In analyzing the claim limitation, the term "scalar vertex data" is misleading in which "scalar" being adjective to "vertex" is used to describe "vertex". However, it is well known in computer graphics art that a vertex of a primitive

is a vector in the two-dimensional or three-dimensional space rather than a scalar. By "scalar vertex data," appellant may mean a scalar for scaling the vertex data. However, Krech teaches scaling the vertex data that inherently involves a scalar for scaling the vertex data and thus the scalar for scaling the vertex data meets the claim limitation of "scalar vertex data." In view of the claim limitation of the "conversion module", Krech teaches the control unit 17 comprising a transform mechanism, a clipping mechanism, a light mechanism, a decomposition mechanism, and a plane equation mechanism for performing transformations on the vertex data such as scaling or moving a vertex in (e.g., three-dimensional) space and therefore the control unit 17 having a tranformation mechenism for scaling the vertex data clearly meets the claim limitation of the "conversion module." Finally, it should be pointed out that scaling the vertex data ("vector vertex data") is well known in the computer graphics art or even the high school geometry, which teaches converting a scalar A to a vector (A, A, A, A) (See line 30 of page 22 and line 1 of page 23 of appellant's specification). A conversion module merely performing such functionality is well known in the computer graphics art or even the high school geometry, not withstanding to a significant portion of the appellant's arguments on the claim limitation of the "conversion module."

On Page 5 in the remarks, the Appellant argued with respect to the claim 24 in substance:

(B) "In rejecting claim 24, the advisory action mimics back the language of the claim but never specifically points out the lighting logic unit or the conversion module. Additionally, the advisory action fails to point out the specific connections between the elements of the claim. For example, in rejecting claim 24, the advisory action states, 'Krech discloses lighting logic unit is

coupled to the multiplicationlogic tmit via a conversion module adapted for converting scalar vertex data to vector vertex data (fig. 5)."

In response to the arguments in (B), the Advisory Action correctly cited Fig. 5, col. 11, line 45 to col. 13, line 15, Fig. 7 wherein these portions of the reference teach the claim limitation set forth in the claim 24. For example, Krech teaches in Fig. 5, col. 11, line 45 to col. 13, line 15, Fig. 7 a control unit logic element 115 (i.e., a lighting logic unit) coupled to the multiplication logic unit (i.e., the MULTIPLIER 55 within the stack 51 of the operating processing element 52 as shown in Fig. 5) via a conversion module (i.e., the control unit 17 of Fig. 5) which operates the vertex data using the control signals or microcode instruction from the logic unit 115 (*See col. 11, line 45 to col. 13, line 15*). The control unit 17 includes among other things, the transform mechanism and light mechanism. In Fig. 5, the TRANSFORM, DECOMP, CLIP, BOW-TIE, LIGHT, FOG mechanisms are clearly shown as being the elements of the conversion module. Thus, the conversion module 17 comprises a transform mechanism (TRANS) 24 for **performing transformations on the vertex data such as scaling or moving a vertex in space**, a decomposition mechanism (DECOMP) for decomposing primitives such as converting a quadrilateral into a triangle and a plane equation mechanism 32 operating on the vertex data via the mathematical operations on the plane equation vector. Krech teaches scaling the vertex data that inherently involves a scalar for scaling the vertex data and the scalar for scaling the vertex data meets the claim limitation of "scalar vertex data." Thus, Krech teaches the TRANS 24 within the unit 17 that converts the vector vertex data using a scalar or **a scalar converted vector**. In summary, the control unit 17 comprising a transform mechanism, a clipping mechanism, a light mechanism, a decomposition mechanism, and a plane equation

mechanism for performing transformations on the vertex data such as scaling or moving a vertex in (e.g., three-dimensional) space meets the claim limitation of the "conversion module."

On Page 3 in the remarks, the Appellant argued with respect to the claim 24 in substance:

(B1) "...a conversion or smearing module 514 coupled between an output of ILU 512 and a second input of MLU 500...the conversion module 514 serves to convert scalar vertex data to vector vertex data."

In response to the arguments in (B1), Appellant stated that a conversion or smearing module 514 coupled between an output of ILU 512 and a second input of MLU 500. In view of the claimed invention set forth in the claim 24 and similar claims, the term "between" is misleading because the claimed invention as recited in the claim 24 recites the claim limitation of the lighting logic unit (e.g., ILU 512) is coupled to the multiplication logic unit (e.g., MLU 500) via a conversion module (e.g., conversion module 514). The term "between" in the summary of invention is not equivalent to the term "via" set forth in the claim 24. Neither can it be construed as being the same to the term "directly between".

Moreover, on the second paragraph of Page 3, it is stated, "the conversion module 514 serves to convert scalar vertex data to vector vertex data." The term "scalar vertex data" is misleading in which "scalar" being adjective to "vertex" is used to describe "vertex". However, it is well known in computer graphics art that a vertex of a primitive is a vector in the two-dimensional or three-dimensional space as opposed to a scalar. By "scalar vertex data", appellant may mean a scalar for scaling the vertex data. Finally, in the Summary of Invention, appellant omits the fact

that the conversion module 514 or the smearing module 514 may be incorporated into MLU 500 and thereby the conversion processing can be performed within a single unit, i.e., MLU 500, which is deemed to be material for patentability of the claim invention set forth in the claim 24. However, a significant portion of the appellant's subsequent arguments is related to a separate "conversion module" in the claim 24.

On Page 7 in the remarks, the Appellant argued with respect to the claim 30 in substance:

(C) "Applicants submit that the 35 U.S.C. 102 rejection against claim 30 and 34 is improper because Krech does not disclose a multiplication logic unit that has a feedback loop coupled to an input of the multiplication logic unit. Accordingly, Applicants submit that the rejection against claim 30 and the corresponding dependent claims should be withdrawn. For simplicity, claim 30 is directly addressed, but the same arguments apply to claim 34."

In response to the arguments in (C), Krech discloses multiplication logic unit has a feedback loop coupled to an input thereof (col. 11, line 45 to col. 13, line 15; fig. 5 and 7). In other words, Krech teaches a vertex looping routine is commenced, which processes data associated with a vertex of the primitive during each loop operation. The appropriate control unit logic element determines via the last vertex bit whether the vertex that was recently operated on in the past by the stack (i.e., the stack 51 having the multiplication logic unit) is the last vertex of the primitive that is currently at issue. Moreover, it is not difficult to find from Krech's Fig. 5, the feedback loop operation (via a plurality of lines that constitutes the feedback loop, wherein the plurality of lines include the flags 131, NEXT_ADDR 108 and INSTR 125) to the MULTIPLIER 55 within the stack 51 of the operating processing element 52 for processing each

of the successive vertices wherein the feedback loop is coupled to the input from the input buffer 77 (See also column 9).

On Page 2 of the reply brief, the Appellant argued:

(E) "At times, the Office Actions are not clear about which elements correspond to which claim limitations, but applicants believe that the chart below accurately sets forth the Examiner's position...."

In response to the arguments in (E), the page 2 of the reply brief *incorrectly* stated Examiner's position regarding the corresponding element in Krech with regards to the claimed element of "multiplication logic unit with the feedback loop" although appellant stated that multiplier 55 of Fig. 5 meets the claim limitation of "multiplication logic unit."

Given the identified elements in Fig. 5 of the prior art teaching, the Examiner has addressed in the Examiner Answer dated 1/27/2005 that Krech's Fig. 5 has the feedback loop operation via a plurality of lines including the line 131, line 148, line 151, line 154, line 108 and line 125 along with a plurality of circuit blocks. The multiplier 55 with the stack of processing elements 51 with he identified feedback loop in Fig. 5 of Krech constitutes the claim limitation of the multiplication logic unit with the feedback loop.

In summary, Krech discloses multiplication logic unit has a feedback loop coupled to an input thereof (col. 11, line 45 to col. 13, line 15; fig. 5 and 7). Krech teaches a vertex ***looping*** routine is commenced, which processes data associated with a vertex of the primitive during each loop operation. The appropriate control unit logic element determines via the last vertex bit whether the vertex that was recently operated on in the past by the stack **(i.e., the stack 51**

having the multiplication logic unit) is the last vertex of the primitive that is currently at issue. Moreover, it is not difficult to find from Krech's Fig. 5, the feedback loop operation (***via a plurality of lines*** that constitutes the feedback loop, wherein the plurality of lines include the flags 131, NEXT_ADDR 108 and INSTR 125) to ***the MULTIPLIER 55*** within the stack 51 of the operating processing element 52 for processing each of the successive vertices wherein ***the feedback loop is coupled to the input from the input buffer 77*** (See also column 9).

On Page 3 of the reply brief, the Appellant argued:

(F) "Krech does not teach applicants' claimed lighting logic unit."

In response to the arguments in (F), The Examiner disagrees with appellant's arguments. These arguments may be misleading as to the patentability of the claimed invention and should be addressed. Appellant argues that Krech's control unit logic 115 is a controller that does not perform the functions of a lighting logic unit. However, Krech's control unit logic 115 issues lighting logic. Appellant's claim element "lighting logic unit" is a unit for providing lighting instructions or logic, rather than also performing the lighting functions within the lighting logic unit itself. A lighting logic unit may provide a lighting logic or instruction to *instruct other units* to perform lighting functions.

In view of the prior art teaching, Krech teaches in Fig. 5, col. 11, line 45 to col. 13, line 15, Fig. 7, any of the following circuit elements, a branch central intelligence 112, a state managmenet address decode 132, a vertex/light counter 139 or a control unit logic element 115 (which includes "a lighting logic unit") is coupled to the multiplication logic unit via a

conversion module (i.e., the control unit 17 of Fig. 5) **which operates the vertex data using the control signals or microcode instruction from the logic unit 115**. The control unit includes among other things, the transform mechanism and light mechanism. In Fig. 5, the TRANSFORM, DECOMP, CLIP, BOW-TIE, **LIGHT**, FOG mechanisms are clearly shown as being the elements of the conversion module. The conversion module 17 comprises a **transform** mechanism (TRANS) 24 for performing ***transformations*** on the vertex data such as scaling or moving a vertex in space, a decomposition mechanism (DECOMP) for decomposing primitives such as converting a quadrilateral into a triangle and a plane equation mechanism 32 operating on the vertex data via the mathematical operations on the plane equation vector.

Therefore, any of the Krech's a branch central intelligence 112, a state managmenet address decode 132, a vertex/light counter 139 or control unit logic element 115 specifically issues control signals or microcode instructions to the control unit 17 having the lighting mechanism 28.

Moreover, as clearly set forth in the context of the Final Rejection of the claim 24, Krech teaches architecturally, the geometry accelerator includes a plurality of processing elements (e.g., an arithmetic logic unit, a multiplier, a divider, a compare mechanism, a clamp mechanism, etc.) and a plurality of control units (e.g., a transform mechanism, a decomposition mechanism, a clip mechanism, a bow-tie mechanism, ***a light mechanism***, a classify mechanism, a plane equation mechanism, a fog mechanism, etc.) that utilize the processing elements for performing data manipulations upon image data. In that ***each of the individual control unit logic elements situated within the control unit logic assists a corresponding control unit in accomplishing branching and indirect addressing***. *Each of the individual control unit logic elements (e.g., the*

lighting logic) is configured to make logical decisions for its respective control unit (e.g., the light mechanism) based upon and as a function of state data, including in the preferred embodiment, two least significant bits (LSBs) of the next address from the current instruction of the ROM, the branch field from the current instruction of the ROM, a condition code from the current instruction of the ROM, *last vertex and light signals from a vertex/light counter indicative of whether or not the current instruction involves the last vertex and last light to be processed in a grouping of vertices/lights associated with a code subroutine*, and the flags from the stack.

In a non-limiting example, In column 9, lines 8-18, Krech discloses the control unit logic element 115 evaluates the last light signal 137 and the last vertex bit 137 and sets the next address 104 so that the current instruction branches to the light control unit 28.

In column 9, lines 60-67 and column 10, lines 1-8 of Krech, it is stated, "A vertex and **light (vertex/light) counter 139** is implemented using any suitable **logic**. The vertex/light counter 139 is designed to count and track vertices as well as lights for a primitive. It produces a last vertex signal 137 and **a last light signal 137** for **the individual control unit logic elements 115** to indicate that the last vertex and last light, respectively, of the primitive has been processed based upon and as a function of the following signals: a flag initialize bit 141 from the ROM 100, next vertex/light signals 142 from the ROM 100, and primitive information 144 (12 bits, of which 4 bits indicate primitive type and **8 bits indicate the number of lights that are turned on**) from the state management address decode mechanism 132, including the primitive type (e.g., point, vector, triangle, quadrilateral, etc.) and the number lights, if any that are turned on.

In column 11, lines 9-20, Krech discloses the branch central intelligence mechanism 112 makes a determination as to whether the primitive should be lighted with the light mechanism 28.

In column 12, lines 56-67, Krech explains how the control unit logic elements 115 works with the branch central intelligent mechanism 112 in terms of the operations of the light logic. It is stated, "the control unit logic element 115 determines the appropriate branch location, i.e., how to modify the next address LSB 104', based upon the next control unit signal 138 from the branch central intelligence mechanism 112."

In column 13, lines 9-27, it is stated, "for each vertex, a light looping routine is commenced, if applicable, which processes data associated with a light(s) of the primitive during each loop operation. As indicated at block 166, **the appropriate control unit logic element 115 determines via the last light bit 137 whether the light that was previously operated on by the stack 51 is the last light of the vertex that is currently at issue**."

In view of the above disclosure of Krech, he clearly teaches a lighting logic unit.

On Page 5 of the reply brief, the Appellant argued:

(G) "Krech does not teach that the 'the lighting logic unit is coupled to the multiplication logic unit via a conversion module."

Responses to the arguments in (F) also apply here because Krech discloses a light logic unit in multiple occasions. According to columns 9-13, each of the elements 115, 112, 132, 139 carries lighting logic and therefore meets the claim limitation of a light logic unit. In addition, appellant mentioned the phrase "coupled" which may mean direct or indirect connectivity

between the claimed elements of the lighting logic unit and the multiplication logic unit. In fact, in Fig. 5 of Krech, each of the elements 115, 112, 132 and 139 having a lighting logic unit is coupled to the stack of processing elements 51 having the multiplier 55 (the multiplication logic unit) via a conversion unit 17 including a lighting transformation 28 and vertex transformation 24.

On Page 5 of the reply brief, the Appellant argued:

(I) "Krech does not teach applicants' claimed multiplication logic unit with a feedback loop."

Given the identified elements in Fig. 5 of the prior art teaching, the Examiner has addressed in the Examiner Answer dated 1/27/2005 that Krech's Fig. 5 has the feedback loop operation via a plurality of lines including the line 131, line 148, line 151, line 154, line 108 and line 125 along with the circuit elements for the multiplication logic unit including the multiplier 55 and therefore these circuit elements and blocks form a feedback loop for the specific circuit block including the multiplier 55. The multiplier 55 within the stack of processing elements 51 has the identified feedback loop.

Appellant further argues that the Examiner does not assert that this feedback loop is *related* to the Krech multiplier 55. However, in column 11, line 44 through column 13, line 15, of Krech, it is clear that this feedback loop is ***specifically related to the stack of the processing elements 52 including the multiplier 55*** and therefore the feedback loop is specifically related to the multiplier 55 because a plurality of circuit elements consitute a feedback loop and appellant's claim invention only recites a broad term of "a feedback loop".

In a non-limiting example, Krech teaches a vertex ***looping*** routine is commenced, which processes data associated with a vertex of the primitive during each loop operation. The appropriate control unit logic element determines via the last vertex bit whether the vertex that was recently operated on in the past by the stack **(i.e., the stack 51 having the multiplication logic unit)** is the last vertex of the primitive that is currently at issue. Moreover, Krech Fig. 5's feedback loop operation having ***a plurality of lines*** constitute the feedback loop and is coupled to ***the MULTIPLIER 55*** within the stack 51 of the operating processing element 52 for processing each of the successive vertices wherein ***the feedback loop is coupled to the input from the input buffer 77*** (See also column 9).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

jcw
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